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High Transconductance Gain Low Voltage Class AB OTA

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***Abstract*—This document presents a low voltage Class AB OTA for high-performance analog circuits. A Flipped Voltage Follower (FVF) variant, known as the Class AB Flipped Voltage Follower, acts as the input stage. It sinks and sources large output currents in comparison to other FVF topologies. The architecture presents a simple structure, using only a few transistors and it requires a low power supply to operate. The OTA experimental results were obtained using the Cadence Virtuoso software for TSMC 180 nm technology. Dc, ac, and transient tests are shown to exhibit the correct performance of the circuit.**

***Index Terms*—CMOS, Class AB circuits, Analog Integrated Circuits, Flipped Voltage Follower, Low-Voltage Circuits.**

I. Introduction

For several years, in the microelectronics industry, it has been necessary to downscale most integrated circuits in order to fit them in state-of-the-art systems, that can function as portable devices. The consequence of this is the use of lower supply voltages nearby the nominal threshold voltages. In turn, mobile telephones make use of these circuits, since they require smaller functional batteries [1].

However, the downscaling process of the transistor also affects the intrinsic gain of the devices themselves [2], but current demand also requires the circuits to perform their tasks quickly, have long input ranges and high linearity at the output [3].

At this point, a circuit building block widely used in analog and mixed-signal design appears, the Operational Transconductance Amplifier (OTA), which acts as a landmark in countless systems thanks to its low power consumption and performance [4].

Unfortunately, not every OTA can solve all situations. There are stage A amplifiers with high linearity (fidelity) at the output, but it has low percentage efficiency. On the other hand, a class B amplifier has high efficiency, but it distorts the signal it receives. An optimal answer for this situation could be, for instance, a stage AB OTA, which, as its name suggests, combines the characteristics of class A and B amplifiers, diminishing the disadvantages of both topologies, offering a highly linear response, moderate efficiency, no-warping effects in the processed signal and, most importantly, large sourcing and sinking output currents.

Current approaches for fashioning high-performance OTAs include complementary differential pairs, floating gates, and folded cascode structures [3].

II. Common OTA Architectures

Several OTA architectures have been designed and implemented over the years, each one of them has considerable advantages for specific case scenarios and important drawbacks.

For instance, a very common topology for low power consumption is the Folded Cascode Amplifier (FC). The FC provides a large DC gain along with a high input range. The PMOS FC is the most used version due to its few dominant poles, a low input common-mode range, and smaller 1/f noise than the NMOS type. However, there are two clear disadvantages in the saturation region. The first is a low transconductance value, which results in low voltage-to-current conversion, making it unsuitable for low voltage applications. The second one is, as the industry demands smaller circuits and chips, power supplies must also be reduced, consequently decreasing the maximum gain of the transistors, whether they have large channels or not [5]. An alternative to improve the FC amplifier's features is by way of multiple-gain structures. However, this technique has an important downside. Huge currents might get duplicated to extra trajectories owing to the current mirrors inside the circuit [6].

An upgrade to the Folded Cascode, is the so-called Recycling Folded Cascode (RFC), which reuses devices in the circuit to perform extra tasks, in other words, idle transistors in the signal path and recycling the input small-signal current. This presents improvements in transconductance value, gain and slew rate [7], however, transconductance in an RFC scheme is proportional to the current mirror gain, known as the K factor, which is not enough to enhance the GBW product and Slew Rate. In addition, if K is increased, so is the power consumption and the non-dominant poles shift at lower frequencies, causing considerable instability [5].
Recently, designers have opted for multi-stage amplifiers due to the escalation of power supplies, leaving aside stacked structures (cascode). These structures, however, require complex frequency compensation. The more stages are added, the harder they are to compensate. The most typical implementa-

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tion is Miller capacitors, but this tends to reduce bandwidth [2].

Another available choice is to make use of the Flipped Voltage Follower to build high-performance OTAs. This architecture has the advantage that the output node has a low impedance, usually of a few tens of ohms. Therefore, the FVF behaves as a source follower and can also sink large amounts of currents due to its shunt feedback between the gate of M1 and node x, being able to adjust the V_{GS} to a correct value to support this. The main drawback is that the cell can only source a current limited to the value I_B from one of the FVF cells when M1 switches off, therefore the circuit operates as a class A amplifier [8].

III. Proposed OTA Architecture

A. Class AB Flipped Voltage Follower

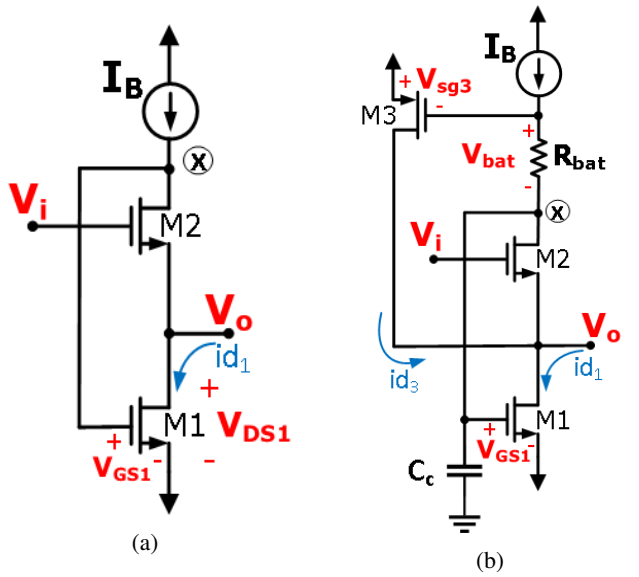

Fig. 1: a) Flipped Voltage Follower and b) Class AB Flipped Voltage Follower

To understand the proposed OTA performance, we must understand the operation of the conventional FVF diagram shown in Fig. 1a.

The FVF is formed by transistors M1 and M2, along with a fixed current source I_B. The input is connected to the gate of M2 and therefore reflects it at the output node V_o, small-signal analysis reveals that the output node has a resistance of approximately $1/g_{m1}g_{m2}r_{o2}$. M1 has a local feedback between its gate and node x that allows the transistor to regulate its gate-to-source voltage at the correct value in order to receive more current if necessary.

Concerning the class AB Flipped Voltage Follower (FVF-AB) shown in Fig. 1b, transistor M1 is capable to provide a large sinking current, whereas M3 is capable to provide a large sourcing current. V_i is interconnected with the gate of M2, which is configured as a source follower. The output node presents the same resistance of $\backsim 1/g_{m1}g_{m2}r_{o2}$ as the typical FVF, maintaining the low resistance characteristic. The resistor R_{bat} sets a voltage V_{bat} between the gates of transistors M1 and M3 in order to place properly saturate them. Considering the voltages sources, the following expression is obtained:

$$V_{supply} = V_{sg3} + V_{bat} + V_{gs1} \tag{1}$$

Where V_{bat}=$I_B R_{bat}$ and uses the same I_B flowing through M2. It is important to remark that the value of I_{D3} can be affected by mismatched values of R_{bat} or voltage supply variations, which can increase power consumption in that transistor. Therefore, the designer can increase or decrease R_{bat} accordingly and obtain the desired values of I_{D3} [8].

The FVF-AB in Fig. 1b requires frequency compensation, according to the analysis in [8], a normally used condition to ensure a sufficient phase margin and guarantee frequency stability is $2GB < \omega_{po}$ [8], thus:

$$C_x/C_L > \frac{4(g_{m1} + g_{m3})}{g_{m2}} \tag{2}$$

B. Operational Transconductance Amplifier based on the FVF-AB

Fig. 2 shows the proposed diagram for class AB operation. Transistors M11, M12, and M13 represent the practical implementation of the ideal I_B sources.

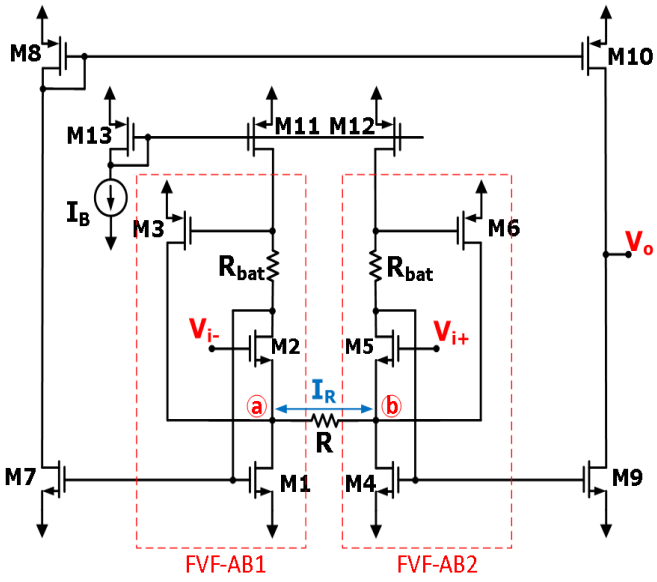

Fig. 2: OTA FVF-AB

The dashed squares highlight the two FVF-AB cells that shape the circuit's input stage. They follow the complementary input voltages at nodes a and b but are altered by the gate-to-source voltage of M2 and M5. Then V_a and V_b generate a tension between the terminals of resistor R and hence a current I_R.

Due to their local feedback, these transistors are capable to adjust their gate-source voltages and sink large differential currents, that are copied to current mirrors M7 and M9. Finally,

M8 and M10 mirror the current in M7 to the output node, thus applying Kirchoff's Current Law, currents belonging to both cells are subtracted (single-ended operation) and a current I_o can be sensed. An equation in terms of I_o and the differential voltages V_{i+} and V_{i-} can be found:

$$I_o = 2\left(\frac{V_b - V_a}{R}\right) = 2\left(\frac{V_{i+} - V_{i-}}{R}\right) = 2\frac{V_i}{R} \tag{3}$$

By working the equation for gm we obtain:

$$g_m = \frac{I_o}{Vi} = \frac{2}{R} \tag{4}$$

A resistance by nature exhibits a linear behavior, in consequence it provides high linearity of the transconductance gain g_m.

Also, note that the minimum supply voltage is given by $V_{SG3,6}$ + V_{bat} + $V_{SG1,4}$; therefore, the rails may be as low as two gate-source voltages if V_{bat} = 0, making it suitable for low voltage environments.

IV. Tests and Results

The OTA FVF-AB was simulated in Cadence using TSMC 0.18 um technology. Nominal threshold voltages are $V_{THN} = 0.45V$ and $V_{THP} = -0.45V$. This circuit was biased with a supply voltage of $V_{supply} = 1.4V$, an $R_{bat} = 7.2K\Omega$, and a current of $I_B = 25\mu A$.

The transistor sizes are $\frac{W}{L}$ = 9/0.36 μm/μm for NMOS and $\frac{W}{L}$ = 27/0.36 μm/μm for PMOS, with $\mu C_{ox} = 395\mu A/V^2$ for NMOS and $\mu C_{ox} = 106\mu A/V^2$ for PMOS.

Fig. 3 shows the transfer function characteristic of the proposed circuit, for different values of R.

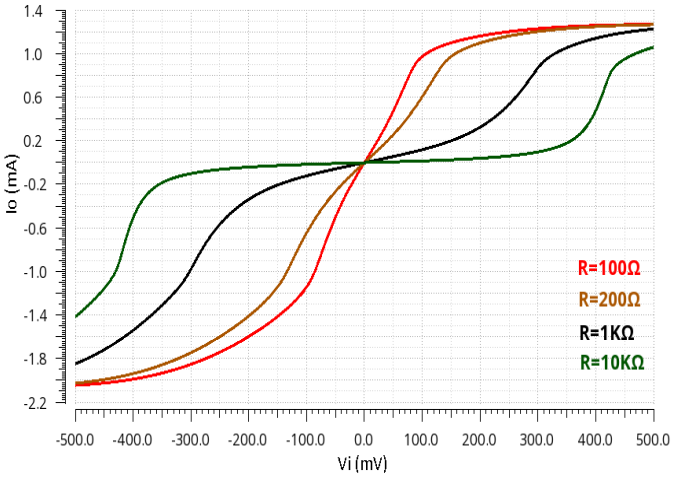

Fig. 3: DC transfer function characteristic

The GB product is defined as g_m/C_L where g_m is 2 mS and C_L was 10pF.

Fig. 4 illustrates the plot obtained from the AC analysis. The obtained zero frequency gain was A_o =39 dB and the Gain–bandwidth product was GBW =18 MHz.

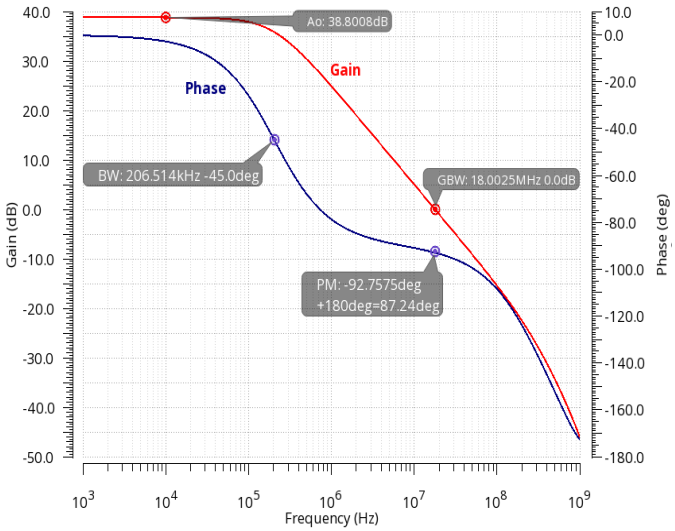

Fig. 4: Gain and Phase

The OTA was tested in a voltage follower configuration with a V_{in} = $0.5V_{pp}$ at 1MHz, with C_L = 10pF. The transient response plot is shown in Fig. 5 with measured values of $SR+$ =16.3 V/μs and $SR-$ =25.3 V/μs.

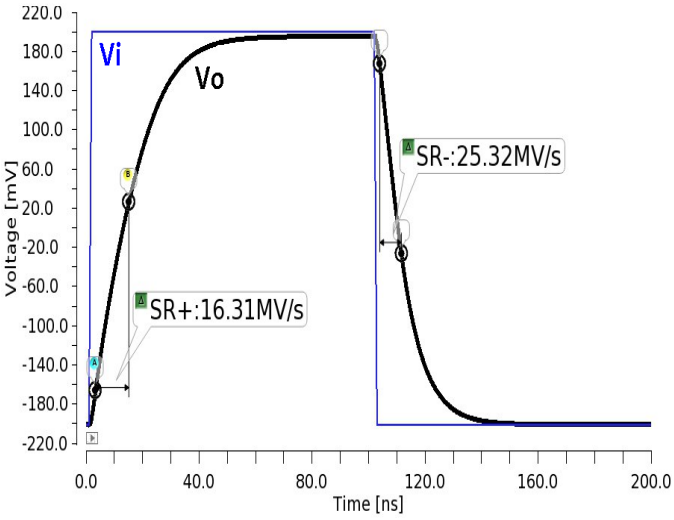

Fig. 5: Transient response.

From (4) the slew rate may be derived using the output current as:

$$SR = \frac{I_o}{C_L} = \frac{2V_i}{RC_L} \tag{5}$$

In this case, the $SR+$ is slightly lower than the $SR-$ since the signal path providing the sourcing current at the load includes the PMOS current mirror formed by M8 and M10.

Table I list the main parameters for the proposed circuit.

TABLE I: OTA FVF-AB main parameters.

Parameter	Value
A_o [dB]	39
BW [kHz]	207
GBW [MHz]	18
Phase Margin [°]	87
I_B [μA]	25
$V_{DD} - V_{SS}[V]$	1.4
$SR+$ [V/μs]	16.3
$SR-$ [V/μs]	25.3
THD [%] ($0.5V_{pp}$ @1KHz)	0.13
C_L [pF]	10

V. Conclusions

A variant of the FVF OTA that operates as a Class AB amplifier was presented. Results indicate that Class AB operation is accomplished due to the FVF-AB cells embedded in the circuit, thus providing large bidirectional output currents and highly linear response. It was biased with a low power supply and the topology demands a little number of transistors, subsequently saving silicon space. Henceforth, the proposed architecture can be used for future works related to high-performance analog applications.

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