2021 18th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE). Mexico city, Mexico. November 10-12, 2021.

Analysis of On-Silicon-Vias for an Advanced RF-CMOS Process: Experimental Characterization and Modeling

Carlos A. Sanabria Díaz
Board Development Group, Intel GDC. Av. del Bosque 1001, El Bajío, 45019 Zapopan, Jal., México, carlos.sanabria.diaz@intel.com

Mónico Linares Aranda
Electronics Department, National Institute for Astrophysics, Optics and Electronics, Luis Enrique Erro No.1, Sta. María Tonantzintla, P. Box 72840, Puebla México. carlos.sanabria@inaoep.mx, mlinares@inaoep.mx

Rogelio M. Higuera González
Tecnológico de Estudios Superiores de Ixtapaluca. Carretera Coatepec s/n Km. 7, San Juan, 56580 Ixtapaluca, México, ing.hgrm@gmail.com

***Abstract*—In this work, a circuit model for interconnection channels with vertical inter-metallic transitions based on the experimental characterization is proposed. The circuit model and extraction methodology was verified using a daisy chain structure manufactured in a 180 nm RF-CMOS process. Both, the parameters extraction methodology and the circuit model were considered for their use in RF applications, whereby they take into account the electromagnetic effects of high frequency. The obtained results show that the proposed circuit model has a maximum average error of 5.06% in magnitude when it is compared with experimental data.**

Keywords—On-Silicon Vias, RF-CMOS process, S-parameters.

I. INTRODUCTION

One of the main trends in the integrated circuit (IC) design is the increases of the operation frequency and integration density with the technological advances. Interconnections in IC designs are negatively affected by the reduction of dimensions in new technologies because the scaling of their cross-sectional area increases resistive losses. The increased integration of devices in ICs places greater demands on the number and length of interconnections, which leads to a higher number of parasitic elements. Additionally, newer CMOS manufacturing processes add more metal layers to meet interconnection requirements in complex ICs [1] and keep the electrical parameters of the global network at optimal values; however, geometric discontinuities are introduced between these metal layers (Fig. 1). These geometrical discontinuities affect the communication channels between the global and local networks through vertical transitions implemented with on-silicon vias (OSV). The OSVs are still considered as RC elements in the design of IC for RF applications [2, 3]. However, with the increment of the frequency due to the technological advances, the inductive behavior of OSVs must be considered as in the case of PCB, RDL and TSV technologies [4, 5, 6].

In [7, 8] an analysis of the electromagnetic behavior was performed for different structures formed by OSV, but it was only limited to full wave simulation results. Nonetheless, the obtained results in those works through a systematic analysis with electromagnetic simulations showed that increasing the connection area in the vertical interconnections by adding OSV does not reduce the associated parasites when a high frequency signal is transmitted through the communication channel. This behavior is different from that observed in classic IC design and it is caused by the high frequency effects, which can be seen as a non-uniformly distributed current in the OSV stacks due to proximity effects in the closer conductors, redistribution of the transmission paths and crowding effects. The observed results for the full wave simulations show that the current tends to confine in the lateral OSVs of the analyzed vertical structures as the frequency increases. These effects are notorious in the electrical characteristics of vertical interconnections, affecting the design of interconnection networks and passive devices such as inductors or resonators, and reducing the integrity of the transmitted signal between global networks and the devices located at the silicon level.

The obtained results of the full wave simulation [7, 8] served of motivation to carry out the corresponding experimental verification and the proposal of an electric modeling that allows the representation of the vertical OSV interconnections for the use in circuit solvers while are considering the high frequency effects. In accordance with the aforementioned, this work presents the manufacture, simulation and modeling of a daisy chain structure with two different OSVs vertical interconnections using an UMC 180 nm technology [9, 10, 11].

II. DESCRIPTION OF PROTOTYPE

Figure 2 shows the designed daisy chain. The structure consists of two OSV stacks with different connection area forming an asymmetric communication channel; in this way this structure allows to represent realistic scenarios where the

978-1-6654-0029-9/21/$31.00 ©2021 IEEE

signal is transmitted through a micro-strip line located in global networks, taken down to local network levels through a strip-line, and finally brought back to a micro-strip line by using an OSV stack.

The OSV stacks used for vertical transitions in the daisy chain for the 180 nm technology are shown in the Fig. 2. It can be observed that the OSV stacks are located between the metal 6 layer (i.e., the top metal layer) and the metal 3, which is commonly used for the devices ports connected to local networks. The width of the daisy chain structures was selected by following the topological rules of the used technology, 20 µm is the maximum allowed to reduce the resistive losses. The short via stack includes 5x34 vias per metal level with a connection area of 3.2x20 µm^2, whereas the long via stack includes 34x34 vias per level of metal with a connection area of 20 x20 µm^2. From Fig. 3 [7] and Table 1 was found that increasing of the number of vias in the arrays beyond a certain amount greatly increases the high-frequency effects and their impact in the parasitic elements, which eventually provides unpractical applications of the analyzed communication channels. For this reason, the lower limit of connection area was 3.2x20 µm^2. Figure 4 shows the layout and a photograph of the manufactured daisy chain prototype in the 180 nm technology.

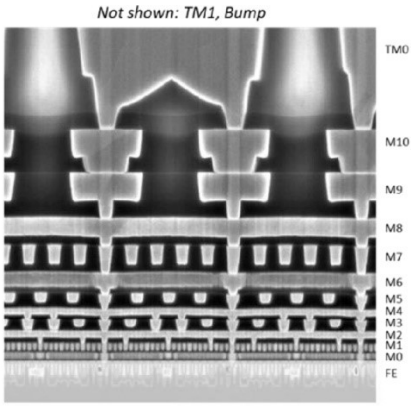

Fig. 1. Intel 10nm BE stack featuring 12 metal layers [1].

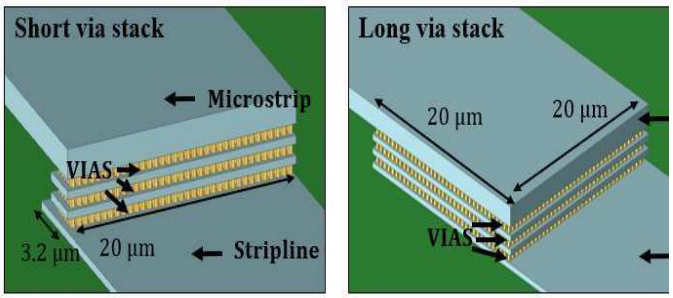

Fig. 2. Perspective view of OSV stacks: (a) Short via stack, (b) Long via Stack.

TABLE I. NUMBER OF VIAS AND AREA (µM^2) FOR DIFFERENT ARRAYS

Arr1(Area)	Arr2(Area)	Arr3(Area)	Arr4(Area)	Arr5(Area)
68 (1.12x20)	170 (3.02X20)	510 (8.4X20)	850 (14X20)	1190 (20X20)

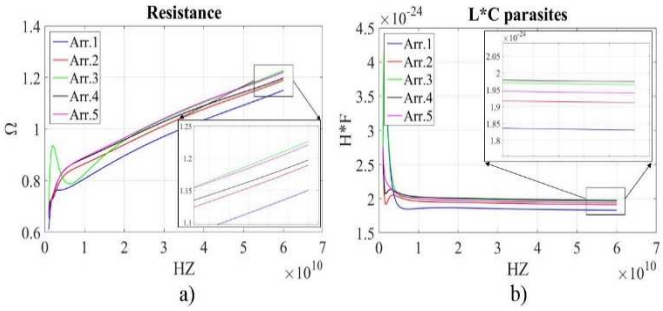

Fig. 3. RLC parasitics of via-arrays in 180 nm: a) Resistance and (b) L*C

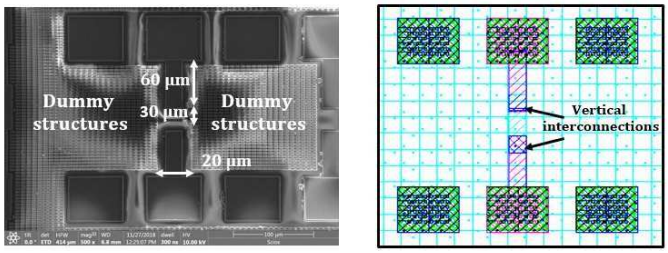

Fig. 4. SEM Picture of the top view and layout for the measured daisy chain prototype.

III. CHARACTERIZATION AND MODELING

The experimental characterization is based in the measurement of the scattering *S*-parameters from the manufactured daisy chain. The *S*-parameters measurements were performed from 70 MHz to 67 GHz by using a VNA and ground-signal-ground coplanar RF I67-GSG-100 micro-probes with a pitch of 100 µm (Fig. 5).

The proposed extraction methodology for the electrical modeling of the daisy chain was based in the de-embedding of the different components of the structure (microstrip, stripline, OVS stacks and pads) helped of electromagnetic simulations. The prototype was implemented through 3-D models and it was simulated by using a full wave solver and considering the material specifications provides by the manufacturer. Aluminum was the metal used to build the interconnections, considering the specification material for the implementation of the final prototype, while silicon dioxide was used as field oxide. An effective permittivity $\mathcal{E}_r$ of 3.82 was used (due to the field oxide is formed by different dielectric layers in the CMOS process) and calculated in function of the nominal values given by the manufacturer. Each one of the daisy chain components (including the OSV stacks) were represented through T-circuit models because is more appropriated for the modeling of short transmission lines. Additionally, the probe pads were modeled with a 34.4fF capacitance based from the data of the manufacturer, while the resistance was extracted from full wave simulations to include the high frequency effects in their values. The pad AC resistance is 0.12 Ω. The values of the electric elements for the circuit representations of the microstrip and stripline were extracted from full wave simulations by using the 3D solver EMpro [12].

Fig. 5. SEM test set-up for the performed measurements

Afterward, the parameters for the T-circuit models were obtained through an optimization in the simulated frequency range by using the circuit simulator ADS [13]. Figures 6 and 7 shows the circuit models extracted from the microstrip and stripline, respectively for the implemented prototype. Additionally, the daisy chain structure was simulated to obtain full wave representations and increases the precision of the extracted circuit models for the OSV stacks. By using the circuit models from the pads, micropstrips and striplines, the electrical representations of the OSV stacks were de-embedding from the full wave simulations of the daisy chain structures and prototype measurement data.

The final model for the measured daisy chain and its electrical values are presented in the Fig. 8. It can be seen, as was expected, that the electrical parameters exhibit a dependency with the frequency while the short via stack has lower values for its LC parasitic elements compared with those shown by the long via stack. Comparing the S parameters obtained from the circuit model and the full wave simulation with the experimental data, a maximum mean error of 5.06% was obtained for the magnitude and 1.89% for the phase, as shown in the figures 9 and 10, respectively.

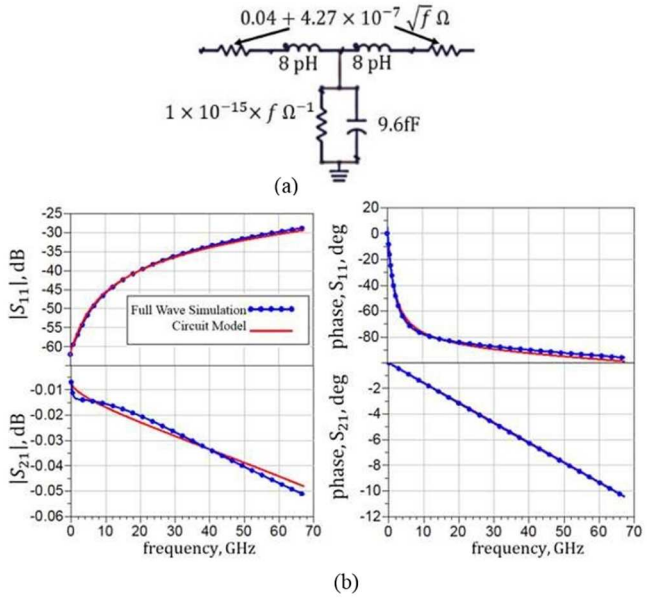

Fig. 6. Microstrip component: (a) Circuit model and (b) Comparison of the *S*-parameters between the full wave and the circuit model.

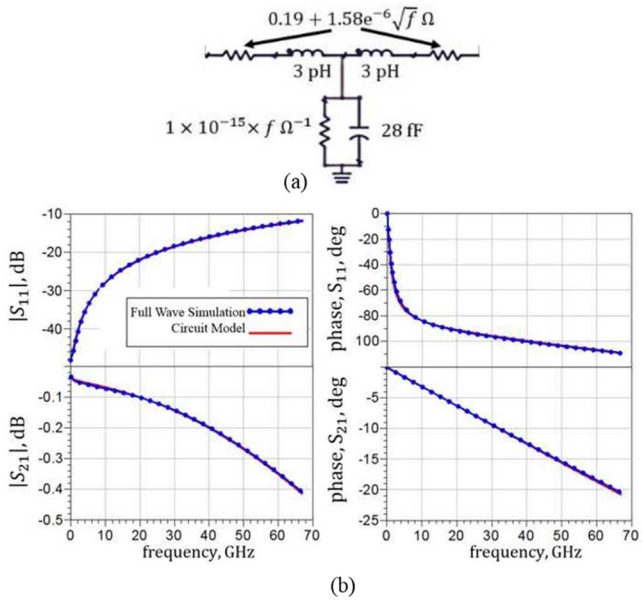

Fig. 7. Stripline component: (a) Circuit model and (b) Comparison of the *S*-parameters between the full wave and the circuit model.

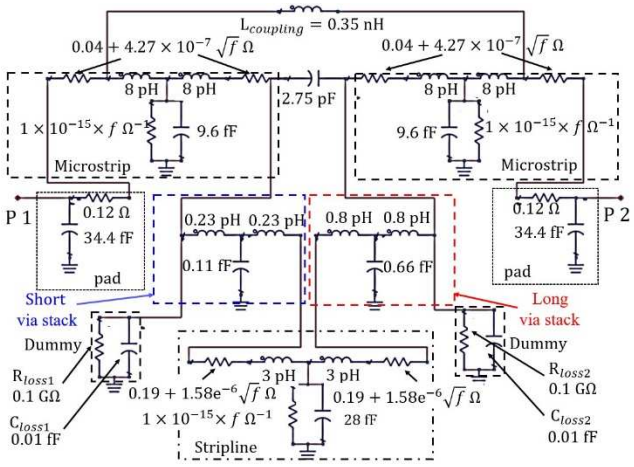

Fig. 8. Proposed circuit model for the prototyped asymmetric daisy chain structure in the 180 nm technology.

It can be seen from Figure 8 that the difference between the return and insertion losses are below of 7.5%, which indicates that the coupling effects and overall losses of the structure are predicted with high accuracy. By other hand, for the phase of the insertion losses, the measured maximum error at high frequencies is 11.2 %. This error indicates that the simulated phase constant, varies from the exhibit in the characterized prototype. This variation is due to the difficulty of accurately representing the effective permittivity of the field oxide in the CMOS processes when the property of the dielectric layers chances between different metal levels in addition to the presence of dummy metals. On the other hand, it can be seen observed that to proposed circuit model, a coupling inductance $L_{coupling} = 0.35$nH was added to model the parasitic path between the input and output of the microstrip lines. The circuit model shows the presence of a lossy capacitive ground connection between the microstrip and the via stacks represented by the

capacitances C_{loss1}, C_{loss2} and the resistors R_{loss1}, R_{loss2}, which model the effect of the metal dummies in the daisy chain. The model also includes a coupling capacitance between the two microstrips with a value of 2.75 pF.

IV. Conclusions

In the present work, communication channels with vertical transitions were modeled by using an asymmetric daisy chain manufactured using an 180nm CMOS process. The maximum average error between the circuit model and the experimental data was below of 5.06% for the return losses (i.e., $|S_{11}|$) when is compared with the experimental data. The measurement data shows that the vertical transition in the manufactured communication channels have LC parasitic element mainly for high frequency applications; this is different to IC low frequency design where parasitic elements for this type of interconnections are considered mainly resistive and are mitigated with the increased of the connection area.

The obtained results show that in high frequency operation, by increasing the connection area of the vertical interconnection not necessarily reduces the value of the associated parasites. Finally, it was observed that the effects of technological scaling introduce higher losses in the field oxide due to the increase in the length and complexity of the OSV stacks with greater connection areas. It can be assumed that in newer technologies, with a large number of metal layers and for applications with higher operation frequencies, the effects of the analyzed parasitic elements will be greater.

Acknowledgment

This work was partially supported by CONACyT-México, under scholarship 281786.

References

[1] F. Griggio, et al., Reliability of Dual-Damascene Local Interconnects Featuring Cobalt on 10 nm Logic Technology. IEEE International Reliability Physics Symposium, pp. 6E.3 1-5, March 2018.

[2] I. Ciofi, et al., RC Benefits of Advanced Metallization Options. IEEE Transactions on Electron Devices, vol. 66, no. 5, pp. 2339-2345, 2019.

[3] J. Jiang, et al., Design optimization for capacitive-resistively driven on-chip global interconnect. IEICE Electron. Express, 12(8):20150111-20150111, 2015

[4] J. Xu, et al. A Survey on Modeling Strategies for High-speed Differential Via between Two Parallel Plates. IEEE EMCSI, Aug 2017, pp. 527-531.

[5] R. Cecchetti, et al. Analytical evaluation of scattering parameters for equivalent circuit of through silicon via array. Electron. Lett., 51(13):1025-1027, 2015.

[6] D. H. Jung, et al. Through silicon via (TSV) defect modeling, measurement, and analysis. IEEE Trans. Compon. Packag. Manuf. Technol., 7(1):138-152, 2017.

[7] C. Sanabria and M. Linares-Aranda. An analysis of On-Silicon-Vias Stack in RF-CMOS Processes. IEEE Lat. Amer. Symp. Circuits and Systems, Feb 2018. pp. 1-4.

[8] C. Sanabria, R. M. G. Higuera and M. Linares-Aranda A simple Model of Inter-Metallic Connections (vias) in CMOS Resonant Rotary Traveling Wave Oscillator (RTWO). Int. Conf. on Electrical Engineering, Computing Science and Automatic Control, Oct 2017. pp. 1-4.

[9] L. Zhang, Z. Li and K. Chakrabarty Built-In Self-Diagnosis and Fault-Tolerant Daisy-Chain Design in MEDA Biochips. IEEE International Test Conference (ITC), Nov 2018. pp. 1-4.

[10] K. Niitsu, et al. Daisy chain transmitter for power reduction in inductive-coupling CMOS link. IEICE Trans. Electron, E90C(4):829-835, 2007.

[11] UMC 0.18 um Mixed-Mode and RFCMOS 1P6M Metal Process Interconnect Capacitance Model. Ver.1.3P.3

[12] EMpro software. (2019) https://www.keysight.com/en/pc-1297143/empro-3d-em-simulation-software

[13] ADS software. (2019) https://www.keysight.com/en/pc-1297113/advanced-design-system-ads

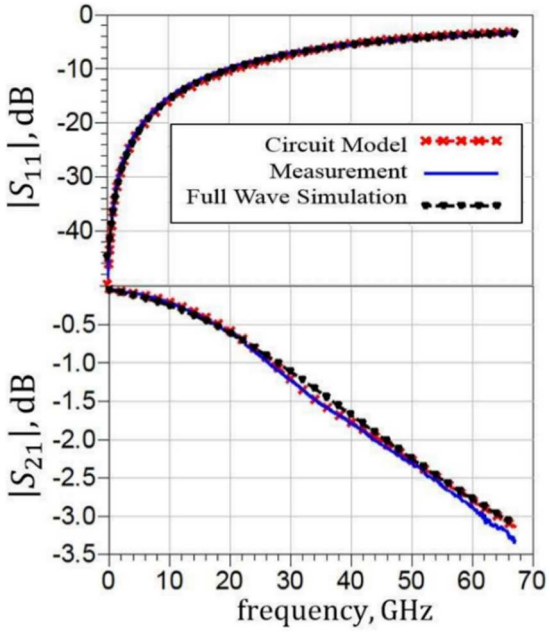

Fig. 9. *S*-parameter comparison: Magnitude

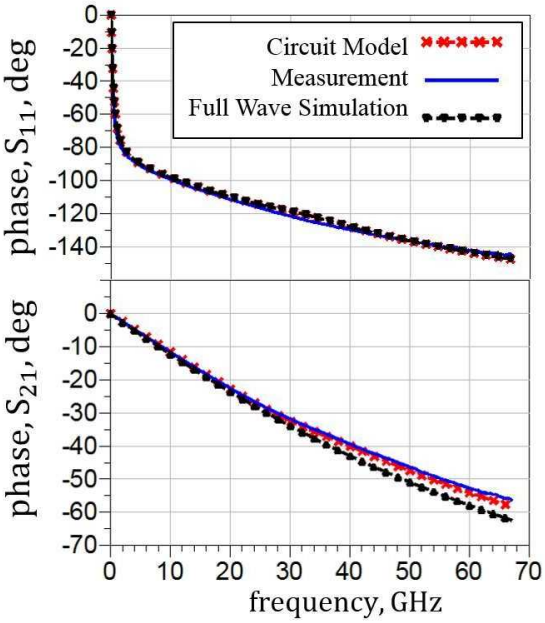

Fig. 10. *S*-parameter comparison: Phase