A Gm-C Notch Filter Implemented With \( g_m \) Over \( I_D \) Technique For Biosignal Acquisition Systems

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Abstract—In this document, we introduce a second order analog Notch Filter to attenuate the frequency of 60 Hz to be implemented in a CMOS integrated circuit, suitable for the acquisition of biosignals, such as electrocorticography. The filter is implemented using four single-stage transconductance operational amplifiers (OTAs). The design of OTAs is done using the gm over id technique. The proposed OTA operates in the saturation region and uses a \( \pm 0.5 \) V supply voltage and dissipates 21 \( \mu \)W of power with 32 dB open loop gain and 4 MHz GBW. The OTA has been used to implement a Gm-C bi-quad filter, which was simulated in the Cadence Virtuoso environment for TSMC 65 nm technology. The simulation results verify the attenuation value at -11 dB for the 60 Hz resonance frequency, as well as an 130 dB CMRR.

Index Terms—Analog Front-End, Analog Notch Filter, bi-quadratic Gm-C filter, Bio-potential acquisition, CMOS, Operational Transconductance Amplifier (OTA), gm/ID methodology.

I. INTRODUCTION

The band reject filter, known as Notch filter (NF), is an essential element for the biosignal acquisition electronic front end (FE), since it eliminates the noise signal generated by the electrical network. The FE determines the performance and quality of a biosignal acquisition system. This interface is made up of some fundamental modules: an instrumentation amplifier (IA), a filter stage (low-pass filter, high-pass filter and NF) and an analog-to-digital converter (ADC) as shown in Fig. 1.

This type of FE is popularly used in biosignal acquisition systems [1]-[3] and these are designed to counteract noise, while extracting signals from the human body. The problems are not only due to the extremely weak characteristics of human body signals, but also to the environment that degrades the quality of the captured signal.

Systems are exposed to ambient noise from various electrical devices that emit interference, including power lines. Therefore, the Notch filter is exclusively responsible for eliminating noise at 60 Hz [4] - [6].

One way to implement the Notch filter is by means of operational transconductance amplifiers (OTA) because it offers a better alternative in filter design without the use of resistors, thus requiring smaller areas of silicon. For biomedical applications, low power consumption circuits are preferred [7]-[10]. Previously, some types of unit gain amplifiers have already been published for the realization of a second order Gm-C filters.

In this work, we design an OTA CMOS with saturated transistors using the \( g_m/I_D \) (\( g_m \) over \( I_D \)) technique. We chose a single stage OTA because we want to reduce the power consumption and the silicon surface required for its implementation. The latter, considering that a less invasive system for the human body is of current relevance.

This document is divided as follows. In the next section we show relevant data on the design of the OTA. Subsequently, the implementation and the results obtained from the Notch filter are discussed, and finally we show our conclusions.

II. OTA DESIGN WITH THE \( g_m/I_D \) METHOD

To design the OTAs that make up the Notch filter, the \( g_m/I_D \) method was used, based mainly on the work presented in [14] and [15].

The methodology was applied to the design of a five-transistor OTA, which is shown in Fig. 2. The transistors are designed to operate in saturation. In addition, the summary of desired performance is summarized in Table 1.

A. Input differential pair design

From GBW specs and \( C_L \) load, the transconductance of the input differential pair is determined by means of the following relationship:

\[
GBW = \frac{g_{m1,2}}{2\pi C_L}
\]

(1)

Resulting \( g_{m1,2} = 130\mu S \). On the other hand, the reference current will generate an equilibrium current in \( M_1 \) and \( M_2 \) of 10\( \mu A \) and so we have
Figure 2. Schematic of a single stage PMOS input OTA.

Table 1
OTA SPECIFICATIONS

<table>
<thead>
<tr>
<th>Concept</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>TSMC 65 nm</td>
</tr>
<tr>
<td>Power Supply</td>
<td>1 V</td>
</tr>
<tr>
<td>Load Capacitor</td>
<td>5 pF</td>
</tr>
<tr>
<td>GBW Product</td>
<td>4 MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>70°</td>
</tr>
<tr>
<td>Open Loop Gain</td>
<td>32 dB</td>
</tr>
<tr>
<td>Input noise</td>
<td>50 uVrms</td>
</tr>
<tr>
<td>Input range</td>
<td>0.1 V – 0.4 V</td>
</tr>
<tr>
<td>Reference Current</td>
<td>10 uA</td>
</tr>
<tr>
<td>Total Current</td>
<td>20 uA</td>
</tr>
<tr>
<td>CMRR</td>
<td>70 dB</td>
</tr>
</tbody>
</table>

\[
\left( \frac{g_m}{I_D} \right)_{1,2} = 13 \text{S/A} \quad (2)
\]

Furthermore, the differential gain is given by:

\[
A_{dc} = \frac{g_{m1,2}}{(g_{ds2} + g_{ds4})} \quad (3)
\]

That means \(10^{(A_{dc}/20)} = 40 \text{V/V}\).

Solving for (2), and using the data in Table 1, we obtain the condition for the output conductance of \(M_2\) and \(M_4\) transistors.

\[g_{ds2} + g_{ds4} < 4 \mu \text{S}\] \quad (4)

Now, we assume that \(M_2\) and \(M_4\) have the same output conductance \(g_{ds2} = g_{ds4} < 2 \mu \text{S}\). So the intrinsic gain will be \((g_m/g_{ds})_{1,2} \geq 63 \mu \text{S/\mu S}\).

Channel length is selected using the intrinsic gain chart \((g_m/g_{ds})\) relative to \((g_m/i_d)\), shown in Fig. 3a. We arbitrarily select the length \(L = 520 \text{nm}\) that gives a \(g_m/g_{ds} \approx 73\) for a \(g_m/i_d = 13 \text{S/A}\), which satisfies the previous equations.

The width of the channel \(W\) is obtained using the chart of \(i_d/W\) vs \(g_m/i_d\), shown in Fig. 3b.

With the previously calculated values for \(g_{m1,2} \text{ y } L_{1,2}\), a current density \(I_D/W \approx 2.041 \mu \text{A/\mu m}\) is observed; thus

\[W_{1,2} = \frac{I_D}{(I_D/W)} \approx 14 \mu \text{m}\] \quad (5)

Figure 3. Charts for PMOS transistors: a) Intrinsic gain \(g_m/g_{ds}\); b) Current density \(I_d/W\); c) \(V_{gs}\) voltage; d) Saturation voltage.
The minimum input signal, before the input pair is out of mirror is limited by the input range and noise specifications. Therefore with $g_{m}/g_{ds}$ figure 4. Charts for NMOS transistors: a) Intrinsic gain $g_{m}/g_{ds}$.

On the other hand, the choice of $g_{m}/I_{D}$ must satisfy:

$$(g_{m})_{1,2} \leq 2\mu S$$

(6)

Now, we assume a relatively large $g_{m}/I_{D} = 15$ [15]. Therefore with $g_{m1,2} = 150\mu S$ and $g_{m}/g_{ds} \geq 75$, from chart in Fig. 4a, we obtain the length of the channel that satisfies these conditions, being $L_{3,4} = 1.95um$.

On the other hand, the choice of $g_{m}/I_{D}$ of the current mirror is limited by the input range and noise specifications. The minimum input signal, before the input pair is out of saturation, is limited by:

$$V_{in, min} = 0.2V \geq -|V_{GS1,2}| + |V_{dsat1,2}| + V_{GS3,4}$$

(7)

$|V_{GS1,2}|$ and $|V_{dsat1,2}|$ are extracted from charts shown in Fig. 3c and Fig. 3d, resulting in $450mV$ and $103mV$, respectively. Substituting into the equation (7), the constraint of $V_{GS3,4}$ for maintain $M3$ and $M4$ in saturation region will be:

$$V_{GS3,4} \leq 0.5V$$

(8)

From value at (8), we observe in chart in Fig. 4b than

$$\left(\frac{g_{m}}{I_{D}}\right)_{3,4} \geq 8.7 S/A$$

(9)

There is a compromise between the input voltage range and noise, where a small $g_{m}/I_{D}$ corresponds to less noise, but this avoids a greater input range of signal oscillation. To correct this, we increase the value of $(g_{m}/I_{D})_{3,4} = 13S/A$. Experimentally, we observed that this satisfies the requirements between the input range and the noise. The width of the transistors $M3$ and $M4$ can be obtained from the current density graph shown in Fig. 4c, where $(I_{D}/W)_{3,4} \approx 1.5uA/um$; thus, the channel width for the current mirror will be $W_{3,4} \approx 8um$.

C. Tail Current Source

To size the tail current transistors $M5$ y $M6$, we start from the Common Mode Rejection Ratio (CMRR). Based in [16], CMRR is defined by:

$$CMRR(dB) = A_{vdc}(dB) - A_{vdc,CM}(dB)$$

(10)

Where $A_{vdc,CM}$ is the common mode DC gain en DC and obtained by:

$$A_{vdc,CM} = \frac{2g_{m1,2}}{1 + 2g_{m1,2}/g_{ds5,6}} \cdot \frac{1}{g_{m3,4}}$$

$$> 10^{\frac{A_{vdc,CM}(dB)}{20}} \approx 0.01V/V$$

(11)

(12)

Therefore, the output conductance of the current source must satisfy:

$$g_{ds5,6} = \frac{g_{m1,2}}{2A_{vdc,CM}g_{m3,4}} < 2.3\mu S$$

(13)

An arbitrary value can be assumed, but relatively large for $g_{m}/I_{D}$ and thus obtain $L_{5}$. We will assume an $g_{m}/I_{D} = 15S/A$. Therefore, it results in $g_{m5,6} = 150uS$ and $g_{m}/g_{ds} \geq 130$. From Fig. 5a, we obtain the length of the channel that satisfies these conditions and $L_{5,6} = 1.56um$.

Additionally, to keep the current source in saturation, the maximum allowable input voltage is given by:

$$V_{in, max} = 0.4V \leq V_{DD} - |V_{GS1,2}| + |V_{dsat5,6}|$$

(14)

The common mode input range CMIR constraint can be written as:
V_{dsat} \leq 95 mV \tag{15}

From the charts in Fig. 5b, the range of \(g_m/I_D\) that satisfies this requirement is \((g_m/I_D)_{5,6} \geq 15 S/A\).

To prevent the current source from operating at the saturation edge, we use for an approximate current density of \(\approx 0.4 \mu A/\mu m\), as shown in chart in Fig. 5c. Consequently, the channel widths of the bias circuit are given by \(W_5 \approx \frac{48}{5} \mu m\) and \(W_6 \approx \frac{24}{5} \mu m\). Table 2 shows a summary of the size of the OTA transistors.

### III. OTA SIMULATION RESULTS

DC analysis of the OTA has been simulated in Cadence Virtuoso in the unity gain configuration, using the circuit configuration shown in Fig. 6. This circuit converts the OTA open loop structure to closed loop unit gain.

The small-signal analysis of the OTA was performed with a 5 pF load capacitor, resulting in an open-loop gain of 32 dB at 10 Hz, while the bandwidth gain product is \(GBW \approx 4 \times 10^6 \). As seen in Fig. 7a and 7b, respectively.

Since the OTA has a single dominant output pole, the specification of the phase margin (PM) is met with a value close to 89°.

### IV. IMPLEMENTATION OF A NOTCH FILTER

The proposed OTA has been used to design a biquadratic Gm-C Notch filter [17] and [18]. The second order notch filter that we implement is shown in Fig. 9.

The transfer function of this second order Notch Gm-C filter is given by:

\[
\frac{V_T}{V_{in}} = \frac{1}{s^2 + \frac{s}{s_{null}} + 1}
\]
To configure the Notch filter with a $Q = 3$, the values of the coefficients of the transfer function presented in (1) were determined. It is proposed that the four cells have the same total transconductance $G_m = 130 \mu S$ and are polarized at $\pm 500$ mV.

From (20) and (21), we obtain $C_1 = 1 \mu F$ and $C_2 = 100 nF$, for a 60 Hz resonance frequency.

The performance of the proposed Notch filter was evaluated by simulations using Cadence Virtuoso for a TSMC CMOS 65 nm technology. The magnitude and phase responses of the small signal analysis of the Notch filter function at 60 Hz are shown in Fig. 10a and Fig. 10b, respectively.

The simulations provided the attenuation value at approximately -11 dB for the 60 Hz resonance frequency.

V. CONCLUSIONS

This document presents a single-stage CMOS OTA design implemented in TSMC 65nm technology, operating in the saturation region. The core consists of a differential pair, a current mirror, and a current source, with a single dominant output pole. This OTA has provided an open loop gain $A_{vdc} = 32 dB$, $GBW = 5 MHz$ and $PM = 89^\circ$. Power consumption was $P_{OTA} = 21 \mu W$, with a power supply of $V_{DD} = -V_{SS} = 500 mV$.

The OTA was used as the main block to implement a Gm-C biquadratic filter, to eliminate the frequency component of the 60Hz power line. This filter used a total of five OTAs that consumed a total power of $P_{NF} = 85 \mu W$ with a power supply of $V_{DD} = -V_{SS} = 500 mV$. This Notch filter can be part of an analog Front End to acquire biosignals.
REFERENCES


