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High-Efficiency DCM Boost Converter for Solar Energy Harvesting

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***Abstract*—A DC-DC boost converter designed in a 0.18µm CMOS process to charge a battery from a 4-series solar cell module is presented in this paper. In order to achieve high efficiency, it works in the Discontinuos Conduction Mode (DCM), and uses two independent control circuits to turn on and off each power switch: a pulse-width modulator to control the low-side power switch M_n and a zero-current detector to control the high-side power switch M_p. The converter provides an output voltage of 3.3V with a ripple lower than 0.5% for an output current I_{load} ranging from 10mA to 50mA. The maximum efficiency achieved is 96.5% for a 2.4V input voltage and I_{load}=50mA.**

***Keywords*— solar energy harvesting, DC-DC boost converter, discontinuous conduction mode (DCM), pulse-width modulation (PWM).**

I. Introduction

The energy provided by solar cells is continuously affected by changes in the incident radiation and temperature and, therefore, except for very specific applications, a power scheme that delivers energy efficiently to the charge and that is robust to changes is required in solar energy powered microsystems [1]. Boost DC-DC converters are usually the preferred option because step up the input voltage and show high efficiency, which is essential in portable applications. This paper focuses on the design of a boost converter and its control system in a 0.18µm CMOS process. The paper is organized as follows. Section II shows the design specifications of the system, according to the energy delivered by the solar module and the battery to be charged. The design of the power plant is presented in Section III, and the design of the control circuitry in Section IV. Section V shows the simulation results and main characteristics of the proposed converter and, finally, conclusions are drawn in Section VI.

II. Design Specifications

A solar cell is an electronic device that converts the incident radiation into electric current through the photovoltaic effect. The solar cells considered in this paper are crystalline silicon cells fabricated at the National Institute for Astrophysics, Optics and Electronics (INAOE) [2]. A single solar cell provides an open circuit voltage V_{oc}=0.58V, a short circuit current I_{sc}=34mA and maximum power P_{max}=14.59mW (at the maximum power voltage V_{mp}=0.46V and I_{mp}=31.83mA). In order to be able to provide the required energy to charge a battery, a module consisting of 4 cells connected in series was considered. Fig. 1 shows the I-V and P-V curves for a single cell and the 4 cells in series. Table I shows the characteristics of the 4-cell module.

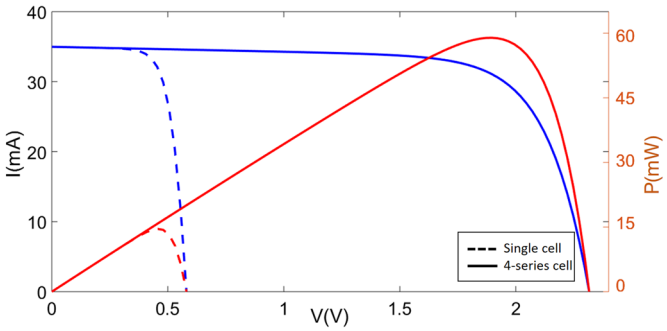

Fig. 1. I-V and P-V curves for a single cell and a 4-cells in series

TABLE I. Connection of 4 Solar Cells in Series

V_{oc}	I_{sc}	V_{mp}	I_{mp}	P_{max}
$2.32V$	$34.98mA$	$1.89V$	$31.23mA$	$58.92mW$

TABLE II. Specifications of the Boost Converter

Parameter	Value
V_{in}	$1.5V - 2.4V$
V_{out}	$3.3V$
V_{rip}	$< 1\%$
I_{load}	$50mA$ fast charge $10mA$ slow charge
Efficiency (η)	>95%

In order to deliver the energy to the battery, the solar module must be connected to a DC-DC converter, whose dynamic behavior is determined by the operating point of the cells, which are expected to work near the point of maximum power (MPP). Therefore, in order to model the solar module, the I-V curve is linearized near the MPP [3]. The model consists of a resistance in series with a voltage source, whose values were estimated to be in this case: $V_g = 3.81\ V$ and $R_g = 61.64\ \Omega$. As for the storage element, a Li-Ion battery is considered, which is modeled as a constant current source I_{load}. During the fast charging mode, I_{load} =50mA and during the slow charging mode I_{load} =10mA. Table II summarizes the design requirements for the DC-DC converter.

III. DC-DC Boost Converter

Fig. 2 shows the basic diagram of a synchronous DC-DC boost converter, where the energy delivered by the source is

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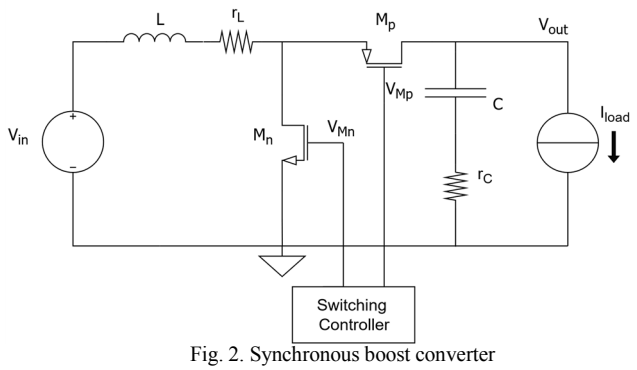

Fig. 2. Synchronous boost converter

first stored in the inductor and then delivered to the load. Both the high-side (M_p) and the low-side (M_n) power transistors work as switches and should never be simultaneously on. Usually the control signal of M_p (V_{Mp}) is derived from the control signal of M_n (V_{Mn}). The time M_n is on is $t_{on} = D_1 T_s$, where T_s is the period of the control signal; the time M_p is on is $t_{off} = D_2 T_s$, and the time both transistors are off is called dead time t_{dead}.

In this paper, the DC-DC converter is designed to work in discontinuous conduction mode (DCM) for all loads, which means that there must always exist a dead time t_{dead} in which the current through the inductor is zero. For this reason, t_{dead} was chosen to be at least 20% of the period. As $T_s = t_{on} + t_{off} + t_{dead}$, the maximum t_{on} is $t_{onMAX} = D_{1max} T_s = 0.8 T_S - t_{off}$.

As already mentioned, the maximum load current considered is i_{load}=50mA. Under these conditions the required inductance is:

$$L = \frac{V_{out} D_{1MAX} (1 - D_{1MAX})^2}{I_{loadMAX} 2 f_s} \quad (1)$$

where $f_s = 1/T_s = 100kHz$, and therefore L=45μH.

The peak current in the inductor i_{pk} in DCM, is given by:

$$i_{pk} = \frac{V_{in}}{L} D_1 T_s \quad (2)$$

There is a compromise between the losses by conduction in the inductor and the switching losses in the power transistors. If the inductance L decreases, so does its DCR series resistance, and therefore the associated conduction losses P_{rL} are reduced. However, as shown in (2), decreasing the inductance causes the maximum current i_{pk} to increase, and the switching losses P_{sw} become dominant. The inductor L=47μH was chosen because it shows the best trade-off between conduction and switching losses. Note that although the design process is here presented as straightforward, an iterative process was actually used to obtain the best trade-off, involving (1) and (2) and power losses P_{rL} and P_{sw}, as proposed in [4].

The size of transistors M_n and M_p was chosen considering the peak current i_{pk}=150mA, and a drop voltage of V_{ds}=20mV:

$$\left.\frac{W}{L}\right|_{n,p} = \frac{i_{pk}}{\mu_{n,p} C_{ox} (V_{gsn,p} - V_{thn,p}) V_{ds}} \quad (3)$$

where V_{gsn}, V_{gsp} are the gate-source voltages of the transistors, $\mu_{n,p}$, C_{ox}, $V_{thn,p}$ are the mobilities, oxide capacitances and threshold voltages, respectively. In order to obtain an output

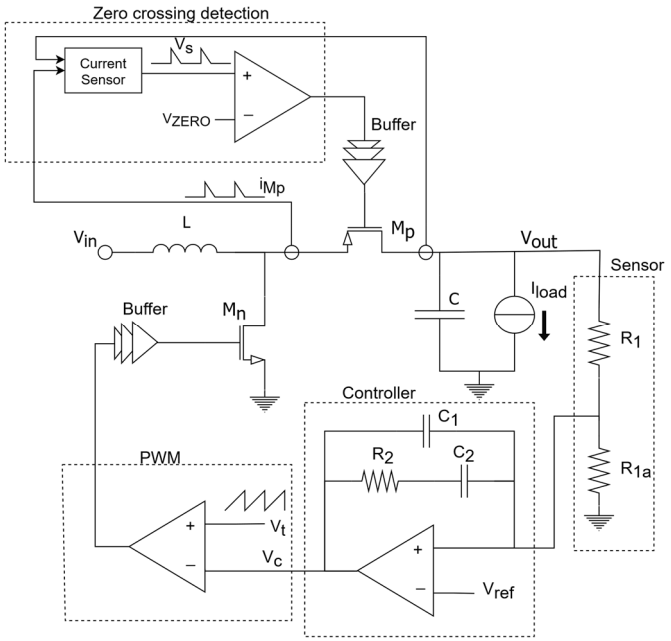

Fig. 3. Control Scheme boost converter

TABLE III. PARAMETERS OF THE DC-DC CONVERTER

L	C	W/L_{NMOS}	W/L_{PMOS}
$47\mu H$	$47\mu F$	$1.8mm/0.34\mu m$	$8.6mm/0.34\mu m$

voltage ripple lower than 1% the load capacitance was $C = 47\mu F$. Table III summarizes the values of each element.

IV. CONTROL SCHEME

In this section, the control scheme of the boost converter is described. PWM control is used with duty cycle of the low-side power switch M_n as control variable. A voltage mode control (VMC) was used because it is simple and robust [5]. Furthermore, as the converter works in DCM, the right half-plane (RHP) zero appears at high frequencies, and the converter can be approximated to a single-pole system, which simplifies frequency compensation [6].

The converter has three independent inputs: variations in the duty cycle d, variations in the input voltage v_{in} and variations in the load current i_{load}. The variations in the output voltage v_{out} can be expressed as a linear combination of the three independent inputs:

$$v_{out}(s) = v_{ref} \frac{1}{H(s)} \frac{T(s)}{1+T(s)} + v_{in} \frac{G_v(s)}{1+T(s)} - i_{load} \frac{Z_{out}(s)}{1+T(s)} \quad (4)$$

The loop gain $T(s)$ is defined as the product of the small signal gains of the direct and feedback loops:

$$T(s) = H(s) G_c(s) G_{vd}(s) G_m(s) \quad (5)$$

where $H(s)$ is the voltage sensor, that is a resistive divider which detects the output voltage, $G_v(s)$ is the input-output transfer function, $G_{vd}(s)$ is the control to output transfer function, $Z_{out}(s)$ the output impedance, $G_m(s)$ is the PWM transfer function and v_{ref} is the reference voltage.

The transfer function without compensation, i.e. $T_{un}(s) = T(s)/G_c(s)$, shows a DC gain of $15.6dB$, which is not high

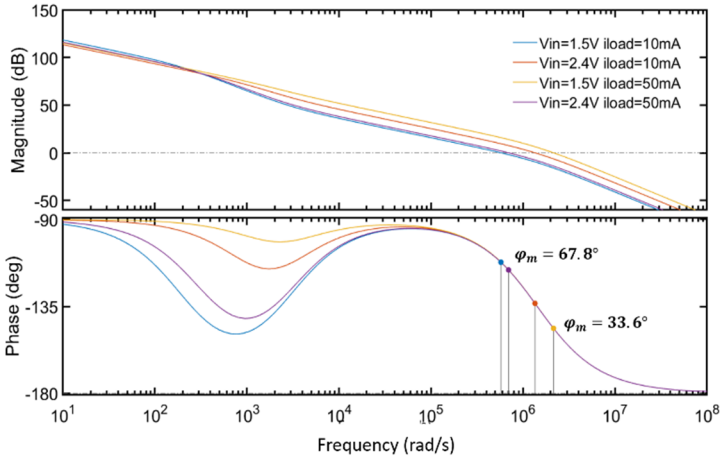

Fig. 4. Loop gain response under different conditions

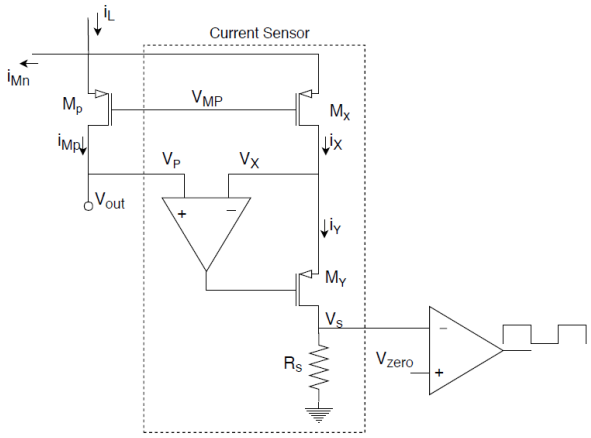

Fig. 5. Zero cross detection circuit

enough for the output voltage v_{out} to accurately follow the reference voltage v_{ref}. For this reason, a controller is required to increase gain, while ensuring stability. As show is Fig. 3, it consists of an error amplifier and a compensation scheme, which correspond to a type II compensator with a pole at the origin, a zero and a pole at a higher frequency. The error amplifier is a 2-stage Miller configuration. Fig. 4 shows the frequency response of the loop gain T(s) under different input and load conditions. It is shown that the phase margin φ_m is higher than 33°, which means that the system is stable.

As for the high-side PMOS power switch, if it is deactivated too early, the current in the inductor does not reach zero, and if, it is turned off too late, the current in the inductor becomes negative. In this work, it is proposed to control M_p just with the zero-current detector scheme show in Fig 5 [7]. The current through the power transistor M_p is copied to M_x and transformed into a voltage by the resistor R_s, whose value is adjusted to obtain an approximate value of $0.5V_{pp}$ in V_s. The comparison between V_s and V_{zero} produces the control signal V_{Mp} of the PMOS transistor, so that the transistor is deactivated when the current through the inductor is almost zero. As shown in Fig. 6, the control signal V_{Mp} is high, and therefore M_p is off, whenever M_n is on. When M_n turns off, the inductor current is forced to flow throw M_p, and therefore it is turned on. The amplifier in the feedback loop is a 2-stage Miller configuration.

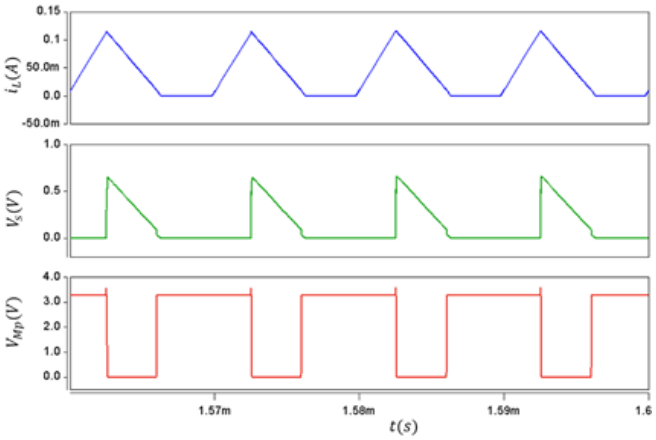

Fig. 6. V_{Mp} control signals working principle

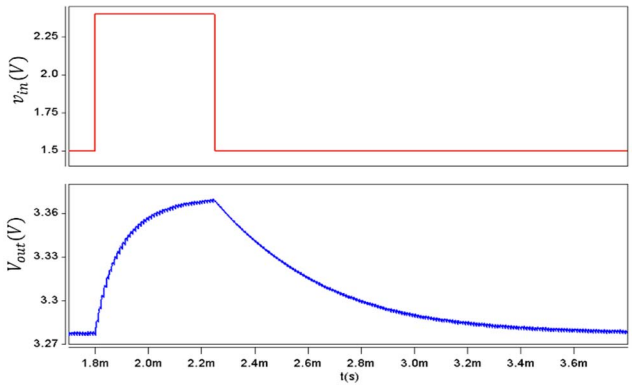

Fig. 7. Transient response to input voltage changes from 1.5V to 2.4V at I_{load} = 10mA

The output comparator also consists of 2 stages. As for the buffer, it consists of 2 CMOS inverters.

V. Simulation Results

Fig. 3 shows the complete scheme of the DC-DC boost converter with PWM control and zero-crossing detection. The output voltage V_{out} is fedback through the resistive divider formed by R_1 and R_{1a}. This voltage is compared with a reference voltage V_{ref} through the error amplifier, to generate the input signal $v_c(t)$ of the PWM modulator, which in turn compares it with a sawtooth signal to control the power switch M_n. The zero-current detector, in turn, senses the current through Mp and turns it on whenever Mn is turned off. It also turns Mp off before the current through the inductor reaches zero, thus resulting in a simple and efficient control scheme.

As mentioned in Section II, the boost DC-DC converter can be used to charge a battery in both the fast charging mode, which requires I_{load} =50mA, and the slow charging mode, which requires I_{load}=10mA. Fig. 7 shows the boost converter response when the input voltage is varied from 1.5V to 2.4V. V_{Mn} and V_{Mp} are the gate voltages of the power transistors M_n and M_p. Under different load current conditions, the worst line regulation was LNR=140mV/V with I_{load} = 50mA. Fig. 8 shows the boost converter response when the load current is varied from 50mA to 10mA. When the converter works under a load current I_{load}=50mA, the maximum current through the

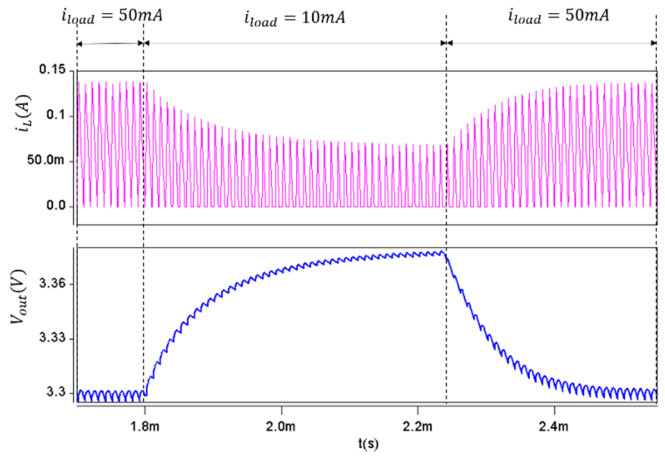

Fig. 8. Transient response to load changes from 50mA to 10mA at v_{in}=2.4

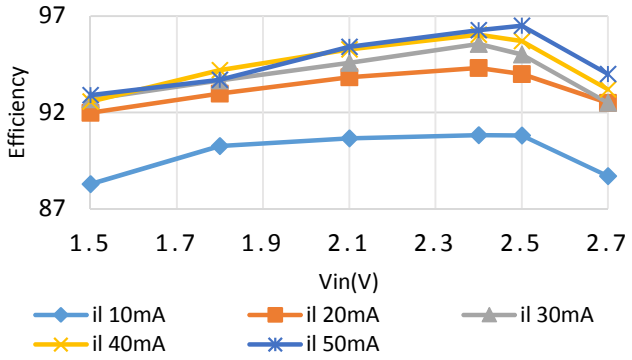

Fig. 9. Efficiency vs. v_{in} for various load currents

TABLE IV. PERFORMANCE COMPARISON BETWEEN DC-DC BOOST CONVERTERS

	This Work	Wang 2014 [4]	Mo 2017 [8]	Hasan 2011 [9]	Lee 2015 [10]
Process	$0.18\mu m$	$40nm$	$0.18\mu m$	$0.18\mu m$	$0.18\mu m$
$V_{inMIN} - V_{inMAX}$	$1.5V - 2.4V$	$0.35V - 0.65V$	$2.68V - 3.3V$	$1.5V - 2.5V$	$1.2V - 1.6V$
V_{out}	$3.3V$	$1V$	$5V$	$3.3V$	$3.3V$
V_{rip}	<0.5%	0.8%	1.93%	< 0.9%	1.1%
LNR (mV/V)	140	76.6	--	17.5	237
LDR (V/A)	2.34@40mA	2.33@9mA	--	0.3@100mA	5.48@90mA
η_{max}	96.5%	95%	91%	94.5%	93%

inductor is i_{pk}=137mA. When the load current changes to 10mA, the current decreases to i_{pk}=70mA. The average value of v_{out} changes from 3.29V to 3.37V in 0.4ms. Under different input voltage conditions, the load regulation in the worst case was LDR=2.34V/A.

The efficiency of the boost converter was obtained under different input voltages and load currents, as shown in Fig. 9. The efficiency decreases as the load current decreases, since it is difficult for the boost converter in DCM to work with low load currents. Also, as the input voltage V_{in} increases, the efficiency under different load conditions is maintained or even increased a little. The converter achieved an efficiency of 96.5% working with I_{load}=50mA and v_{in}=2.4V.

Finally, a comparison between state-of-the-art DC-DC boost converters and the proposed scheme is shown in Table IV. The proposed DC-DC boost converter presents low output voltage ripple when compared with other implementations. It also shows high efficiency because of the simplicity and effectiveness of the control blocks, which generate the control voltage of the high-side and low-side power transistors in an independent manner, thus saving logic circuitry.

VI. CONCLUSIONS

A boost converter to charge a battery from 4-series solar cells was designed in 0.18-μm CMOS technology. A pulse-width modulator was used to control the low-side power transistor, whereas the high-side switch was controlled with just a zero-current detector. The designed converter adjusts to changes in the input voltage and load current to maintain an output voltage of 3.3V with a ripple voltage of up to 0.5%. In particular, the converter has a line regulation of LNR=140mV/V and a load regulation of LDR=2.34V/A, considering a range of input voltages of 1.5V-2.4V, and a range of load currents of 10mA-50mA. The maximum efficiency of the converter was 96%, and in general was higher than 88% under all established load and voltage input conditions. The lowest efficiency was obtained when the converter worked with the lowest load current (slow charging mode).

ACKNOWLEDGMENT

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